	Type	Hits	Search Text	DBs	Time Stamp
1	BRS	1636	(CMOS with logic) same (DRAM or memory)	USPAT; US-PGPUB	2002/06/23 12:58
2	BRS	3	((CMOS with logic) same (DRAM or memory)) and ((hemispherical adj grained adj polysilicon) or HSG)	USPAT; US-PGPUB	2002/06/23 12:59
3	BRS	283	(CMOS with logic) same (DRAM or memory)	EPO; JPO; DERWENT; IBM_TDB	2002/06/23 12:58
4	BRS	0	((CMOS with logic) same (DRAM or memory)) and ((hemispherical adj grained adj polysilicon) or HSG)	EPO; JPO; DERWENT; IBM_TDB	2002/06/23 12:59
5	BRS	937	(DRAM or memory) and ((hemispherical adj grained adj polysilicon) or HSG)	USPAT; US-PGPUB	2002/06/23 12:59

DOCUMENT-IDENTIFIER: US 5858831 A
TITLE: Process for fabricating a high performance logic and embedded dram
devices on a single semiconductor chip

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ABPL:
A process for creating a region of high performance logic devices, and a region
of low cost **memory** devices, on a single semiconductor chip, has been developed.
The process features **CMOS logic** devices, comprised of polycide gate structures,
residing on a thin silicon dioxide gate insulator layer. An N type polysilicon
layer, used as part of a polycide structure, is used with the N channel CMOS
devices, while a P type polysilicon layer, is used with the P channel CMOS
devices. **DRAM memory** devices are comprised of polycide gate structures,
featuring only an N type polysilicon layer, on a silicon dioxide gate insulator
layer, that is thicker than the gate silicon oxide layer used with the high
performance logic devices. A minimum of additional photolithographic masking
procedures is used to improve the performance of the logic region, one mask to
allow specific polycide gate structures to be created with either P type or N
type polysilicon, and another additional mask used to allow different gate
insulator layers to be formed in each specific region. A large angle, ion
implantation procedure, is used to form lightly doped source and drain regions,
under the silicon nitride spacers on the sides of polycide gate structures, in
both logic and **DRAM memory** regions.

BSPR:
Efforts have been ongoing by the semiconductor industry, in

attempting to
incorporate both logic and **memory** requirements on a single semiconductor chip.
Dennison, in U.S. Pat. No. 5,292,677, describes a process for integrating
complimentary metal oxide semiconductor, (CMOS), devices, with dynamic random
access **memory, (DRAM)**, devices, on a single semiconductor chip. However that
invention does not share as many processing steps needed to realize significant
cost reductions, nor does it offer a process needed for high performance logic
devices. This invention will describe an integrated process, which features
high performance CMOS devices, realized via many innovations such as the use of
gate insulator layers, thinner than the gate insulator layers used for the **DRAM**
devices. It will also feature the use of conductive silicide layers for source
and drain regions of the CMOS devices, formed using a process sequence that
reduces a possible bridging mechanism between gate structures and substrate.
In addition this new process, for forming high performance **logic,** and embedded
memory devices, on a single semiconductor chip, will be practiced using many
process sequences, shared by both type devices, with the addition of only two
photolithographic masking procedures, added to the **CMOS logic** process sequence,
which enables improved performance of the **logic** region to be realized while and
still achieve cost reductions.

BSPR:
It is an object of this invention to provide a process for fabricating high
performance **CMOS logic** devices, and embedded **DRAM memory** devices, on the same
semiconductor chip.

BSPR:
In accordance with the present invention a fabrication process is described for

integrating high performance **CMOS logic** devices, and embedded **DRAM memory** devices, on a single semiconductor chip. After formation of P well regions for both the embedded **DRAM** devices, and N channel CMOS devices, as well as the formation of an N well region, for the P channel CMOS devices, a deep, N type layer, is formed in the semiconductor substrate, in the **DRAM** region, to isolate a subsequent **DRAM** cell from the underlying substrate. After creation of a thin gate insulator layer, for the **CMOS** devices, and a thicker gate insulator layer, for the **DRAM** devices, an undoped polysilicon layer is deposited, followed by creation of shallow trench isolation regions, used to separate subsequent P channel and N channel **CMOS** devices, in the **logic** region of the semiconductor chip, as well as separating the **memory** region of embedded **DRAM** devices, from the high performance **logic** region comprised of **CMOS** devices. A process sequence, using only one photolithographic masking procedure is next used to N type dope the polysilicon region to be used for the **DRAM** devices, as well as the polysilicon region, to be used for N channel CMOS, while doping the polysilicon region used for the P channel CMOS devices, P type. Silicon nitride capped, polycide gate structures, comprised of titanium silicide on N type, or P type polysilicon, are next formed, followed by creation of silicon nitride spacers, on the sides of the polycide gate structures, only in the **CMOS logic** region of the semiconductor chip. An ion implantation procedure, using a large tilt angle, and low dose, is used to create N type, lightly doped source and drain regions, under silicon nitride spacers, for N channel CMOS devices, followed by a higher dose, lower tilt angle, procedure, used to create N type,

heavily doped source and drain regions, for the same N channel CMOS device. A similar ion implantation sequence is used to create the P type, lightly doped source and drain, and the P type, heavily doped source and drain regions, for the P channel CMOS devices. Metal silicide is next formed on the exposed source and drain regions, in the CMOS region, of the semiconductor chip.

BSPR:
A silicon oxide layer is next deposited, planarized, and removed in areas between polycide gate structures, in the **DRAM** region. After formation of silicon nitride spacers, on the sides of the polycide gate structures in the **DRAM** region, ion implantation procedures are performed, using a large tilt angle implant, to create N type, lightly doped source and drain regions, again under silicon nitride spacers. Polysilicon plugs are next formed between polycide gate structures, in the **DRAM** region of the semiconductor chip. Another silicon oxide layer is deposited and patterned to create a storage node opening, exposing the top surface of a polysilicon plug. A stacked capacitor structure is formed in the storage node opening, in the silicon oxide layer, overlying and contacting the polysilicon plug, in the **DRAM** region. An insulator layer is next deposited, followed by photolithographic and dry etch procedures, used to open contact holes and via holes to the stacked capacitor, and bit line regions, in the **DRAM** region, as well as to the gate, and source and drain regions in the **CMOS logic** region. Metal deposition, followed by removal of unwanted metal, are employed to form the metal contact structures, in the contact and via holes, followed by additional metal deposition and patterning, used to create metal interconnect structures,

for both the **DRAM** **memory** devices, and for the **CMOS logic** devices.

DRPR:
FIGS. 1-20, which schematically, in cross-sectional style, illustrates key stages of fabrication used to construct the **CMOS** devices, used for high performance **logic,** and the embedded **DRAM** devices, used for low cost **memory,** on a single semiconductor chip.

DEPR:
FIG. 1, shows region 50, of semiconductor substrate 1, to be used for fabrication of high performance **CMOS logic** devices, while region 60, of semiconductor substrate 1, will be used for embedded **DRAM** **memory** device. A P type, single crystalline silicon substrate 1, having a <100> crystallographic orientation is used. A photolithographic masking procedure, using photoresist shape 3, is used as a mask to allow N well region 4, to be formed only in openings in photoresist shape 3, in logic region 50, via ion implantation of phosphorous and arsenic. A high energy boron, ion implantation procedure, allows formation of P well regions 2, in regions of semiconductor substrate 1, underlying photoresist shape 3, in **DRAM** region 60, as well as in an area of **logic** region 50, with P well regions 2, needed for N channel **CMOS** devices. The high energy boron implants are located deep into semiconductor substrate 1, in regions unprotected photoresist, under N well regions 4, and do not influence device characteristics. Photoresist shape 3, is removed using plasma oxygen ashing and careful wet cleans.

DEPR:
FIG. 2, shows the formation of a deep, N type region 6, used to isolate **DRAM** region 60, from semiconductor substrate 1. This is

performed using thick
photoresist shape 5, greater then 5.0 uM in thickness, protecting logic region
50, from a high energy phosphorous ion implantation procedure, performed at an
energy between about 1 to 2 MeV, at a dose between about 1E12 to 1E13
atoms/cm.sup.2, creating isolating deep N type region 6. In addition, a
threshold adjust, ion implantation procedure, using boron, at an energy between
about 1 to 10 KeV, and at a dose between about 1E11 to 1E12 atoms/cm.sup.2, is
used to alter the channel doping characteristics near the surface of
semiconductor substrate 1, in **DRAM** region 60. The threshold adjust region,
created in **DRAM** region 60, is not shown in the drawings, but is used to create
DRAM devices with higher threshold voltages than the N channel **CMOS** devices
that will be subsequently created in **logic** region 50.

DEPR:
A silicon nitride layer 14, is next deposited using LPCVD or PECVD procedures,
to a thickness between about 1000 to 1500 Angstroms. A photoresist shape, (not
shown in the drawings, and the second mask added to the process for **logic**
performance improvement), is used as a mask to allow removal of silicon nitride
layer 14, in **DRAM** region 60, and in the area of **logic** region 50, to be used for
N channel **CMOS** devices. After removal of the masking photoresist shape, via
plasma oxygen ashing and careful wet cleans, a POCl.sub.3 procedure is used to
dope exposed regions of undoped polysilicon layer 9a, and creating N type
polysilicon layer 9b, in **DRAM** region 60, as well as in **logic** region 50, to be
used for N channel **CMOS** devices. The furnace POCl.sub.3 procedure was chosen
for polysilicon doping, rather then an ion implantation procedure, which can
damage underlying gate insulator layers. The result of

this procedure is
schematically shown in FIG. 6. A silicon oxide layer 15,
is thermally grown,
on N type doped, polysilicon layers 9b, to a thickness
between about 300 to 600
Angstroms, allowing removal of silicon nitride layer 14,
via use of a hot
phosphoric acid solution. A blanket, boron ion
implantation procedure is used,
at an energy between about 0.5 to 1 KeV, and at a dose
between about 1E15 to
5E15 atoms/cm.sup.2, resulting in exposed, undoped
polysilicon layer 9a, in an
area of **logic** region 50, to be used for subsequent P
channel **CMOS** devices, to
be converted to P type polysilicon layer 9c, with a surface
concentration
between about 0.75 to 1.25E21 atoms/cm.sup.3. The N type
dopant concentration
for N type polysilicon layer 9b, is between about 0.75 to
1.25E22, and
therefore even if N type polysilicon layer 9b, was
subjected to the boron ion
implantation procedure, the level of P type compensation
still would not be
enough to convert N type polysilicon layer 9b. This is
schematically shown in
FIG. 7.

DEPR:
After removal of silicon oxide layer 15, via a wet etch
procedure, a titanium
nitride layer 16, is deposited using R.F. sputtering
procedures, to a
thickness between about 80 to 120 Angstroms, followed by
the deposition of a
titanium disilicide layer 17, deposited using R.F.
sputtering procedures to a
thickness between about 750 to 1250 Angstroms, and finally
a silicon nitride
layer 18, is deposited using PECVD or LPCVD procedures, to
a thickness between
about 1500 to 2500 Angstroms. The result of these
depositions is schematically
shown in FIG. 8. Photoresist shapes 19, are next employed
as a mask, allowing
polycide gate structures to be formed. Polycide, (titanium

disilicide on
polysilicon), structures, capped with silicon nitride, are formed via
anisotropic RIE procedures, using CHF.sub.3 as an etchant for silicon nitride
layer 18, and using Cl.sub.2 as an etchant for titanium disilicide layer 17,
for titanium nitride layer 16, and for the polysilicon layers. Polycide
structures in **DRAM** region 60, and in the area of the **logic** region 50, used for
N channel **CMOS** devices, are comprised with N type polysilicon layer 9b, while
the polycide structure, in the area of the **logic** region 50, used for P channel
CMOS devices, is comprised with P type polysilicon layer 9c. This is
schematically shown in FIG. 9.

DEPR:
A thick silicon oxide layer 34, is deposited using LPCVD or PECVD procedures,
to a thickness between about 5000 to 10000 Angstroms. Photoresist shape 35, is
used to allow storage node openings 36, to be formed in thick silicon oxide
layer 34, via a selective, anisotropic RIE procedure using C.sub.2 F,
--CF.sub.4 --O.sub.2, as an etchant. The selectivity of the etchant does not
allow polysilicon plugs 33, or silicon nitride layer 18, exposed at RIE
endpoint, to be etched. The thickness of silicon oxide layer 34, will
influence the height, and therefore the capacitance, of a subsequently formed
capacitor structure, to be located in storage node openings 36. This is
schematically shown in FIG. 17. After removal of photoresist shape 35, via
plasma oxygen ashing and careful wet cleans a thin, N+ polysilicon layer 37, is
deposited via LPCVD procedures, to a thickness between about 500 to 700
Angstroms. A titanium nitride, or tungsten nitride layer, can be used to
replace polysilicon layer 37, if desired. However since

polysilicon layer 37,
will be used for the storage node of a capacitor structure, another option is
the use a hemispherical grained, (**HSG**), polysilicon layer, to increase surface
area of the storage node structure. Next the capacitor dielectric layer 38, is
created. Capacitor dielectric layer 38, can be an Oxynitride--Nitride --Oxide,
(ONO), layer, or any insulator with a high dielectric constant. If ONO is the
choice it can be created by first thermally growing a silicon oxide layer, at a
thickness between about 10 to 20 Angstroms, on the surface of polysilicon layer
37, followed by the deposition of a silicon nitride layer, using LPCVD or PECVD
procedures, at a thickness between about 50 to 80 Angstroms. An oxidation
procedure, in an oxygen -stream ambient, at a temperature between about
750.degree. to 900.degree. C., converts the surface of the silicon nitride
layer to a oxynitride. The resulting ONO layer 38, has a equivalent silicon
oxide thickness between about 25 to 55 Angstroms. Another option for the
capacitor dielectric layer 38, is a Ta.sub.2 O.sub.5 layer, a barium strontium
titanate, (BST), layer, or a lead zirconium titanate, (PZT), layer, at an
equivalent silicon oxide thickness between about 25 to 55 Angstroms. A CMP
procedure is next performed, resulting in polysilicon, storage node layer 37,
and capacitor dielectric layer 38, residing only in storage node openings 36.
This is shown schematically in FIG. 18.

CLPR:
16. A method for fabricating a high performance **CMOS logic** region, and a low
cost **DRAM memory** region, on the same semiconductor chip, using an integrated
fabrication process, comprising the steps of:

CLPR:

23. The method of claim 16, wherein said N type, lightly doped source and drain regions, formed in said P well region of said **CMOS logic** region, and in said P well region of said **DRAM memory** region, are formed via ion implantation of arsenic or phosphorous, at an energy between about 30 to 50 KeV, at a dose between about 1E13 to 3E13 atoms/cm.sup.2, and at an implant angle between about 30.degree. to 45.degree..

CLPV:
removing said second silicon oxide layer from said **DRAM memory** region, resulting in said silicon oxide plugs, in regions between said polycide gate structures, in said **CMOS logic** region;